REMARKS

Claims 4-83 are pending in this application. Claims 4-7, 9, 29-31, 36-42, and 53 have been rejected. Claims 8, 10, 32-35 and 43-52 have been objected to. Claim 4 has been amended. Claims 8, 10, 16, 21, 26, 30-32, 34-35, 43-45, and 49 have been rewritten. Claims 54-83 have been added.

Claims 4-7, 9, 29-31, 36-39, and 53 have been rejected under 35 U.S.C. § 102(e) as being anticipated by *Tsen* (U.S. Patent No. 5,936,906). Claims 40-42 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsen in view of *Banks* (U.S. Patent No. 6,602,614). These rejections are respectfully traversed.

Tsen at best merely discloses a primary cells array 100 that includes flash cells that store multilevel digital data. A word decoder 102 selects flash cells using word lines WL. A bitline decoder 104 selects bitlines BL connected to the flash cells. ('906 patent, col. 2, l. 60-col 3, l. 5.) "[A] reference cells array 110 is electrically coupled to the primary cells array 100 via the word lines [WL] for sharing the word lines [WL]." ('906 patent, col. 3, lns. 6-8.) The reference latch cells are set at threshold voltages by applying reference signals to the corresponding word line that is selected by the word line decoder 102. ('906 patent, col. 3, l. 66-col. 4, l. 16.) During reads from the memory cells, the current from the read memory cell is compared in the sense amplifier 120 to the reference currents stored in the reference cells array 110. ('906 patent, col. 4, lns. 38-59.)

Banks at best merely discloses a multibit per cell electrically alterable non-volatile memory system 100 that includes an MxN array of non-volatile cells. Word lines 104 connect the memory cells. Bitlines 106 connect columns of memory cells. The output of sense amplifiers 112 coupled to the bitlines and a reference voltage detect a voltage. A decode/encode circuit 114 decodes the data bits which are latched in an input/output, N-bit latch/buffer 116. ('614 patent, Fig. 5, col. 8, l. 43-col. 9, l. 7.)

Claim 4 has been amended to recite in pertinent part a plurality of multidimensional memory arrays. Neither *Tsen* nor *Banks* disclose or even suggest individually or in combination a plurality of multidimensional memory arrays as recited in amended claim 4. Lacking the disclosure of this claim feature, the references of record, individually or in combination, do not render claim 4 unpatentable. Because claims 5-7, 36-42, and 53 depend, directly or indirectly,

on claim 4, for similar reasons claims 5-7, 36-42 and 53 are not rendered unpatentable by the references of record. Therefore, it is respectfully submitted that claims 4-7, 36, 42 and 53 are patentable over the references of record.

Claim 30 has been merely rewritten in independent form, and thus its scope remains precisely the same as originally filed.

The rejection of claim 30 is respectfully traversed. Neither *Tsen* nor *Banks* disclose or even suggest, individually or in combination "the reference cells are disposed at approximately linearly spaced locations along the at least one common line" as recited in rewritten claim 30. As understood, *Tsen* and *Banks* are silent about locations of the reference cells. Accordingly, there is no motivation to modify *Tsen* or *Banks* to include reference cells disposed at approximately linearly spaced locations as recited in rewritten claim 30. Lacking the disclosure or suggestion of this claim feature, none of the references of record, individually or in combination, render claim 30 unpatentable. Therefore, it is respectfully submitted that claim 30 is patentable over the references of record.

Claim 31 has been merely rewritten in independent form, and thus its scope remains precisely the same as originally filed.

The rejection of claim 31 is respectfully traversed. Neither *Tsen* nor *Banks* disclose or even suggest, individually or in combination, "the reference cells are disposed at approximately geometrically spaced locations along the at least one common line" as recited in rewritten claim 31. As understood, *Tsen* and *Banks* are silent about locations of the reference cells. Accordingly, there is no motivation to modify *Tsen* and *Banks* to include reference cells disposed at approximately geometrically spaced locations along the at least one common line as recited in rewritten claim 31. Lacking the disclosure or suggestion of this claim feature, the references of record, individually or in combination, do not render claim 31 unpatentable. Therefore, it is respectfully submitted that claim 31 is patentable over the references of record.

Claims 8, 10-28, 32-35, and 43-52 have been objected to for being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Allowable claims 8, 10, 16, 21, 28, 32, 34-35, 43, 44, 45, and 49 have been merely rewritten in an independent form pursuant to the Examiner's request, and thus their scope remains precisely the same as originally filed.

Claims 11-15 depend, directly or indirectly, on claim 10, which has been rewritten in independent form, and thus claims 11-15 are no longer dependent on a rejected claim.

Claims 17-20 and 22-27 depend, directly or indirectly, on claim 16, which has been rewritten in independent form, and thus claims 17-20 and 22-27 are no longer dependent on a rejected claim.

Claim 33 depends on claim 32, which has been rewritten in independent form, and thus claim 33 is no longer dependent on a rejected claim.

Claims 46-48 depend, directly or indirectly, on claim 45, which has been rewritten in independent form, and thus claims 46-48 are no longer dependent on a rejected claim.

Claims 50-52 depend, directly or indirectly, on claim 49, which has been rewritten in independent form, and thus claims 50-52 are no longer dependent on a rejected claim.

Therefore, withdrawal of the objection to claims 8, 10-28, 32-35, and 43-52 is respectfully requested.

Claims 54-83 have been added to include claim coverage to which applicant believes it is entitled.

It is submitted that claims 4-83 are allowable, and allowance and issuance of this application is respectfully requested.

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Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned APPENDIX – MARKINGS TO SHOW CHANGES MADE.

Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. **07-1896, referencing 2102397-991720.**

Dated: June 17, 2002

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APPENDIX – MARKINGS TO SHOW CHANGES MADE

4. (amended) A data storage system comprising:

a plurality of multidimensional memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells.

8. (amended) [The] A data storage system [of claim 4, further] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a second address decoder operatively coupled to the at least one common line, the second address decoder configured to receive an input address and select one or more common lines.

10. (amended) [The] A data storage system [of claim 4, further] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a reference generator coupled to the at least one memory decoder and the reference array, the reference generator configured to provide a first set of signals to the reference array and the bias signals to the at least one memory decoder.

16. (amended) [The] A data storage system [of claim 4,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells,

wherein each memory array includes a plurality of segments, each segment including P rows by Q columns of memory cells.

21. (amended) [The] A data storage system [of claim 4, further] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of current sinks disposed along each of the at least one common line.

28. (amended) [The] A data storage system [of claim 4,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells,

wherein each common line is driven from both sides of a memory array.

30. (amended) [The] A data storage system [of claim 29,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells,

wherein the reference cells are disposed at approximately linearly spaced locations along the at least one common line.

31. (amended) [The] A data storage system [of claim 29,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells,

wherein the reference cells are disposed at approximately geometrically spaced locations along the at least one common line.

32. (amended) [The] A data storage system [of claim 29, further] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, each reference array includes a plurality of reference cells, each reference cell operative to provide one reference signal; and

a plurality of reference lines coupled to the plurality of reference cells, wherein resistance of the reference lines is approximately matched to resistance of common lines.

34. (amended) [The] A data storage system [of claim 29,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

wherein the reference array includes a plurality of reference cells, each reference cell operative to provide one reference signal,

wherein each reference signal is generated by averaging outputs from two or more reference cells.

35. (amended) [The] A data storage system [of claim 4, wherein] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells;

the reference array includes[:] a plurality of reference cells operative to provide the reference signals, wherein at least one of the reference signals is generated by extrapolating outputs from two reference cells.

43. (amended) [The] A data storage system [of claim 42,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation,

each driver comprising a voltage comparator coupled to the associated bit line and a reference source, the voltage comparator configured to compare a voltage on the bit line and one of the reference signals from the reference array and to provide a comparison result,

wherein each driver further comprises:

a multiplexer operative to receive the reference signals from the reference array and to provide one of the reference signals to the voltage comparator.

44. (amended) [The] A data storage system [of claim 40,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation,

wherein each driver is associated with one memory cell during programming, and wherein each driver further comprises: an inhibit circuit operative to enable or inhibit programming of a particular memory cell coupled to the associated bit line.

45. (amended) [The] A data storage system [of claim 40,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation,

wherein each driver is associated with one memory cell during programming, and

wherein each driver further comprises:

control circuitry configured to generate a first status signal indicative of a particular memory cell coupled to the associated bit line being placed in a program inhibit mode.

49. (amended) [The] A data storage system [of claim 40,] comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells;

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells; and

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation,

wherein each driver includes control circuitry configured to generate a third status signal indicative of a particular memory cell coupled to the associated bit line being incompletely programmed.